## Name:

| Problem | Points | Score |
| :---: | :---: | :---: |
| 1 a | 10 |  |
| 1 b | 10 |  |
| 1 c | 10 |  |
| 1 d | 10 |  |
| 2 a | 10 |  |
| 2 b | 10 |  |
| 2 c | 10 |  |
| 3 a | 10 |  |
| 3 b | 10 |  |
| 3 c | 10 |  |
| Total | $\mathbf{1 0 0}$ |  |

## Notes:

1. The exam is closed book / closed notes. Students are allowed a copy sheet - only ONE standard US-size (8.5" x 11") sheet of paper - on which they can write relevant information such as theorems.
2. Please show ALL work. Incorrect answers with no supporting explanations or work will be given no partial credit.
3. If I can't read or follow your solution, it is wrong, and no partial credit will be given PLEASE BE NEAT!
4. Please indicate clearly your answer to every problem.
5. There is sufficient space after each problem to write your solution. In case you need extra paper please see the instructor.
6. Calculators of any kind are not allowed.

## Problem No. 1:

Your electronics company has been contracted to design and manufacture radars for the latest F16 aircraft. This radar detects enemy aircraft by sending a sequence of electromagnetic pulses. If a pulse sequence of either 110 or 010 is returned, it signals presence of an enemy aircraft. You have to implement this radar as an iterative network.
a) Start your design with a state diagram for the typical cell of the iterative network. Draw the corresponding state table.

## Solution:

b) Using the implication charts method, get rid of all redundant states in your state table. [Hint: The minimized network should have at most four states.]

## Solution:

c) Using the state assignment guidelines, assign state variables to these states and construct a state table in terms of the state variables.

## Solution:

d) Derive the corresponding state and output equations for a D Flip-flop implementation.

## Solution:

## Problem No. 2:

The 74S163 counter has the following function table -

| Control Signals |  |  |  | Next State |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CLEAR | LOAD | PT | $\mathbf{Q}_{\mathrm{D}}{ }^{+}$ | $\mathbf{Q}_{\mathrm{C}}{ }^{+}$ | $\mathbf{Q}_{\mathrm{B}}{ }^{+}$ | $\mathbf{Q}_{\mathrm{A}^{+}}$ |  |
| 0 | X | X | 0 | 0 | 0 | 0 |  |
| 1 | 0 | X | $\mathrm{D}_{\mathrm{D}}$ | $\mathrm{D}_{\mathrm{C}}$ | $\mathrm{D}_{\mathrm{B}}$ | $\mathrm{D}_{\mathrm{A}}$ |  |
| 1 | 1 | 0 | $\mathrm{Q}_{\mathrm{D}}$ | $\mathrm{Q}_{\mathrm{C}}$ | $\mathrm{Q}_{\mathrm{B}}$ | $\mathrm{Q}_{\mathrm{A}}$ |  |
| 1 | 1 | 1 | present state +1 |  |  |  |  |

Implement the following Moore machine with four states given by BA, an input X and an output $Z$ using such a counter chip and external logic.

a) Draw the next state table to reflect the various counter inputs to implement this network.

## Solution:

b) Draw corresponding K-maps and derive the equations for the counter inputs LOAD, PT and $D_{B}$.

## Solution:

c) This network is used to drive a 74178 4-bit PIPO shift register, such that the serial input $\mathrm{SI}=\mathrm{Z}$, shift enable $\mathrm{SH}=\mathrm{B}$ and load enable $\mathrm{L}=\mathrm{A}$. The parallel inputs to the register are fixed at 0101, and the initial value loaded in the register is 0000. If the control network starts in state S0, give the values in the shift register for an input sequence of $X=1110$.

The 74178 function table is as follows -

| Control Signals |  | Next State |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathbf{S H}$ | $\mathbf{L}$ | $\mathbf{Q}_{A}{ }^{+}$ | $\mathbf{Q}_{\mathrm{B}}{ }^{+}$ | $\mathbf{Q}_{\mathrm{C}}{ }^{+}$ | $\mathbf{Q}_{\mathrm{D}}{ }^{+}$ |
| 0 | 0 | $\mathrm{Q}_{\mathrm{A}}$ | $\mathrm{Q}_{\mathrm{B}}$ | $\mathrm{Q}_{\mathrm{C}}$ | $\mathrm{Q}_{\mathrm{D}}$ |
| 0 | 1 | $\mathrm{D}_{\mathrm{A}}$ | $\mathrm{D}_{\mathrm{B}}$ | $\mathrm{D}_{\mathrm{C}}$ | $\mathrm{D}_{\mathrm{D}}$ |
| 1 | X | SI | $\mathrm{Q}_{\mathrm{A}}$ | $\mathrm{Q}_{\mathrm{B}}$ | $\mathrm{Q}_{\mathrm{C}}$ |

[Hint: This can be done independent of part b)].

## Solution:

## Problem No. 3:

Design a network to perform the following add-subtract operation: $R=X+Y-Z$ where R, X, Y and Z are binary numbers.
a) Implement the add-subtract network for the case where $X Y Z$ are two-bit numbers and $R$ is a three-bit number using two full-adders and three full-subtracters. Draw a block diagram of your design.

$$
r_{2} r_{1} r_{0}=x_{1} x_{0}+y_{1} y_{0}-z_{1} z_{0}
$$

## Solution:

b) The system in part a) uses two and three bit numbers. What are the maximum and minimum possible values for such an operation using positive arithmetic? What are the maximum and minimum possible values using 2's compliment signed arithmetic?

## Solution:

c) If $R, X, Y$ and $Z$ are $n$-bits long, the network should be implemented as an iterative network. Show the block diagram of a typical cell for such a network with appropriately labelled inputs, outputs and state variables. Do not derive any equations.

## Solution:

