**ECE 2313: Electrical Engineering Science I**

# Laboratory No. 9: Transient RESPONSE

The goal of this laboratory is to reinforce your understanding of the transient response of DC circuits. We will accomplish this using series and parallel RLC circuits. For each of these tasks, except Task No. 4, you must develop an analytic expression for the voltage or current, demonstrate your analytic result matches your Multisim simulation of the circuit, and further demonstrate that an implementation on the Digilent board matches your solution. You can reference results in your textbook or other textbooks. However, be sure to include enough details that the analysis can be understood.

In your lab report, include a description of your analysis, plots of the expected outcomes, and plots of what you observe on the Digilent board.

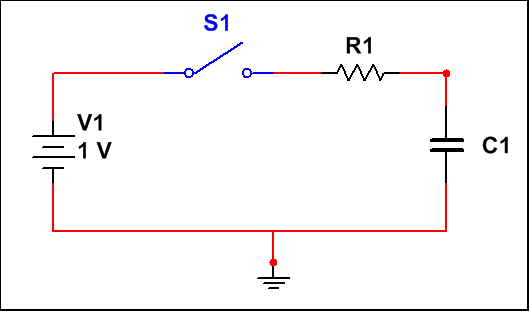


Figure 1. A series RC circuit is shown. Assume zero initial conditions.

**Task 1: Series RC and RL Circuits**

Assume the switch, S1, is closed at t = 0. Following the steps above, design the circuit shown in Figure 1 (e.g., find the values of R1 and C1) such that the voltage across the capacitor, VC1 reaches 90% of its final value within 100 msec. Plot the resulting voltage as a function of time for the range [0, 1 sec], validating your design.

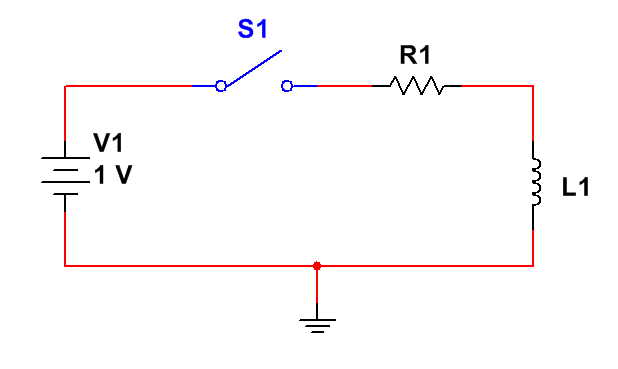


Figure 2. A series RL circuit is shown. Assume zero initial conditions.

Similarly, for the circuit shown in Figure 2, design the circuit such that the current through the inductor, IL1, reaches 90% of its final value within 100 msec. Plot the resulting current as a function of time for the range [0, 1 sec].

**Task 2: Parallel RC and RL Circuits**

Repeat the steps in Task No. 1 for the parallel RC and RL circuits shown in Figure 3 and Figure 4. Assume the switch, S1, has been connected for a very long time and is opened at t=0. As before, plot the voltage across the capacitor and the current through the inductor.

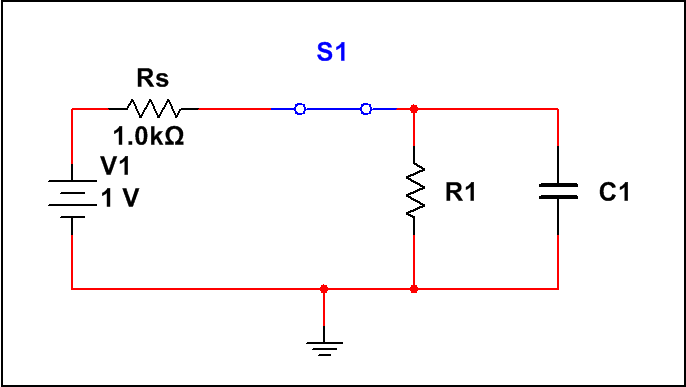


Figure 3. A parallel RC circuit is shown. Assume switch S1 has been connected for a long time and is opened at t=0.

**Task 3: Series and Parallel RLC Circuits**

In Figure 5 and Figure 6, series and parallel RLC circuits are shown. In lecture, we discussed that each of these circuits can exhibit three types of behavior: Case 1: overdamped; Case 2: underdamped; and Case 3: critically damped. For this task, we will focus on the voltage across the capacitor. Again, we will use a 90% criterion: design the circuit so that the voltage reaches 90% of its final value at 100 msec.

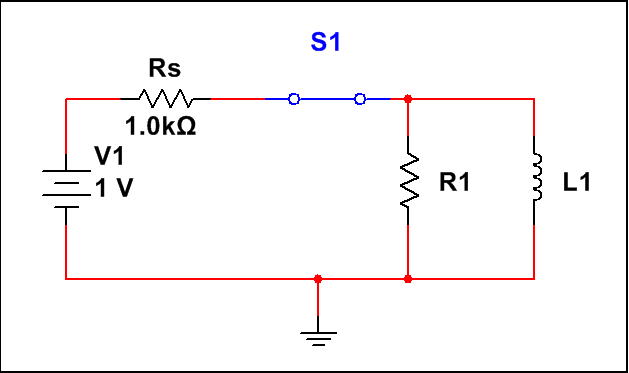


Figure 4. A parallel RL circuit is shown. Assume switch S1 has been connected for a long time and is opened at t=0.

However, repeat this process for each of the three cases for each circuit. Plot your results in a way that clearly demonstrates you have met your design constraints. For the underdamped case, use the envelope of the waveform for the 90% criterion.

**Task 4: Impulse Response**

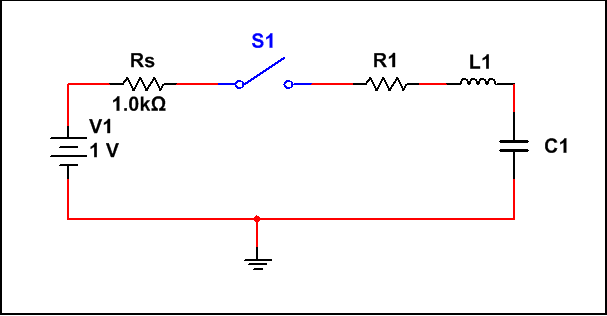


Figure 5. A series RLC circuit is shown. Assume zero initial conditions and that switch S1 is closed at t=0.

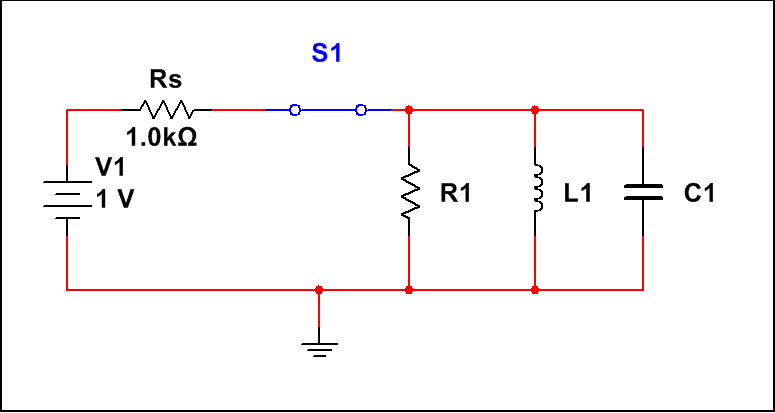


Figure 6. A parallel RLC circuit is shown. Assume switch S1 has been connected for a long time and is opened at t=0.

For this task, we will use the design of your circuits in Task No. 3 that achieves an underdamped response. Replace the combination of the voltage source, series resistance and switch with a pulse generator. Generate a periodic pulse train that has a frequency of 1 second and a duty cycle of 10% (e.g., switches from 0 to 1 V at t=0, and holds that value for 100 msec, then repeats this every 1 second).

Compare the results of your Multisim simulation with the results of your Digilent hardware implementation. Demonstrate that these are comparable.

Finally, analyze and explain the results you are seeing. Do they make sense? If so, why? Explain these results in qualitative terms, but use the knowledge you have gained from the first three tasks to explain how the components are charging, discharging, and corrupting the pulsed input.

**Summary:**

In this laboratory, we have demonstrated how to characterize the transient behavior of circuits. We have demonstrated very simple, but useful configurations of RC, RL and RLC circuits.

In Task No. 4, we have given you a glimpse of things to come. The pulse train you are applying to the circuit could very well represent the problem of transmitting a digital signal over a long cable or equivalent communications channel. The circuit can be viewed as a filter and can represent a model of how the communications channel distorts the pulse. What can we do to overcome this? What aspects of the pulse cause the distortion?

In ECE 3512, you will also learn that as we shorten the duration of the pulse and increase its amplitude the output you are observing, in the limit, becomes the circuit’s impulse response. We can determine a lot about the behavior of the circuit from its impulse response (including the frequency response of the system). The methods for measuring the impulse response (Task No. 4) and the step responses (Tasks No. 1-3) are very practical ways to measure and characterize the behavior of a circuit or system.